

# DATA SHEET

## **74LVC2244A**

Octal buffer/line driver; with 30  $\Omega$   
series termination resistors; 5 V  
tolerant input/output; 3-state

Product specification  
Supersedes data of 2002 Dec 13

2004 Apr 07

## Octal buffer/line driver; with 30 $\Omega$ series termination resistors; 5 V tolerant input/output; 3-state

### 74LVC2244A

#### FEATURES

- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power consumption
- Direct interface with TTL levels
- Inputs accept voltages up to 5.5 V
- Integrated 30  $\Omega$  termination resistors
- Complies with EIA/JESD36
- ESD protection:  
HBM EIA/JESD22-A114-B exceeds 2000 V  
MM EIA/JESD22-A115-A exceeds 200 V.
- Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$  and  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$ .

#### DESCRIPTION

The 74LVC2244A is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 V or 5 V devices. In 3-state operation outputs can handle 5 V. These features allow the use of these devices as translators in a mixed 3.3 V and 5 V environment.

The 74LVC2244A is an octal non-inverting buffer/line driver with 3-state outputs. The 3-state outputs are controlled by the output enable input pins  $1\overline{\text{OE}}$  and  $2\overline{\text{OE}}$ . A HIGH on pin  $n\overline{\text{OE}}$  causes the outputs to assume a high-impedance OFF-state. Schmitt-trigger action at all inputs makes the circuit highly tolerant for slower input rise and fall times. The 74LVC2244A is designed with 30  $\Omega$  series termination resistors in both HIGH and LOW output stages to reduce line noise.

#### QUICK REFERENCE DATA

GND = 0 V;  $T_{\text{amb}} = 25\text{ }^{\circ}\text{C}$ ;  $t_r = t_f \leq 2.5\text{ ns}$ .

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
$t_{\text{PHL}}/t_{\text{PLH}}$	propagation delay nAn to nYn	$C_L = 50\text{ pF}$ ; $V_{\text{CC}} = 3.3\text{ V}$	3.1	ns
$C_I$	input capacitance		4.0	pF
$C_{\text{PD}}$	power dissipation capacitance per buffer	$V_{\text{CC}} = 3.3\text{ V}$ ; notes 1 and 2	8	pF

#### Notes

1.  $C_{\text{PD}}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).

$$P_D = C_{\text{PD}} \times V_{\text{CC}}^2 \times f_i \times N + \Sigma(C_L \times V_{\text{CC}}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

$C_L$  = output load capacitance in pF;

$V_{\text{CC}}$  = supply voltage in Volts;

$N$  = total load switching outputs;

$\Sigma(C_L \times V_{\text{CC}}^2 \times f_o)$  = sum of the outputs.

2. The condition is  $V_I = \text{GND}$  to  $V_{\text{CC}}$ .

Octal buffer/line driver; with 30  $\Omega$  series termination resistors; 5 V tolerant input/output; 3-state

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## ORDERING INFORMATION

TYPE NUMBER	PACKAGE				
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE
74LVC2244AD	-40 °C to +125 °C	20	SO20	plastic	SOT163-1
74LVC2244ADB	-40 °C to +125 °C	20	SSOP20	plastic	SOT339-1
74LVC2244APW	-40 °C to +125 °C	20	TSSOP20	plastic	SOT360-1
74LVC2244ABQ	-40 °C to +125 °C	20	DHVQFN20	plastic	SOT764-1

## FUNCTION TABLE

See note 1.

INPUT		OUTPUT
$\overline{nOE}$	$nAn$	$nYn$
L	L	L
L	H	H
H	X	Z

## Note

1. H = HIGH voltage level;  
L = LOW voltage level;  
X = don't care;  
Z = high-impedance OFF-state.

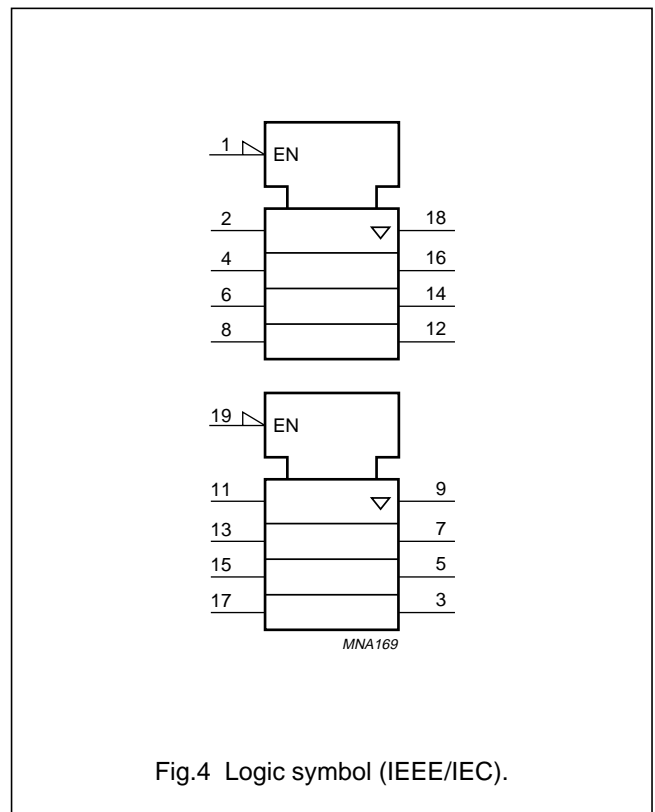
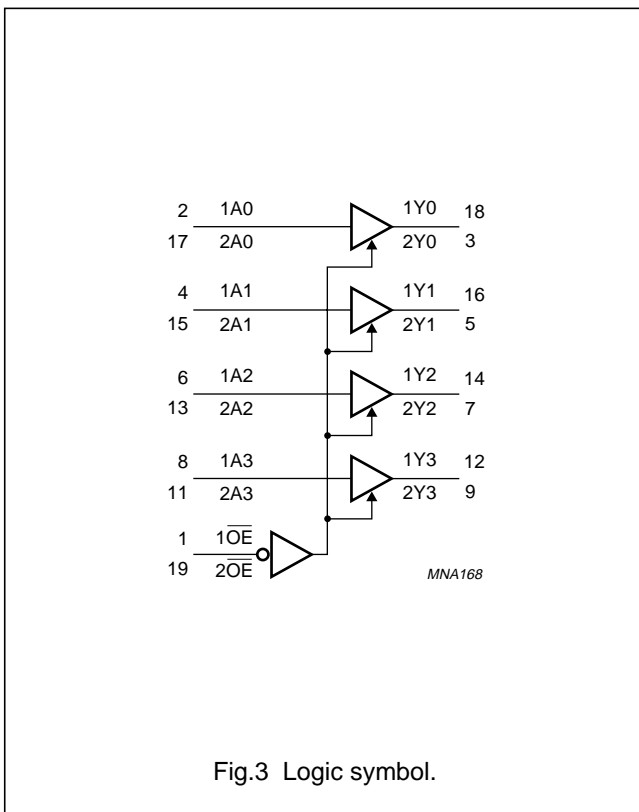
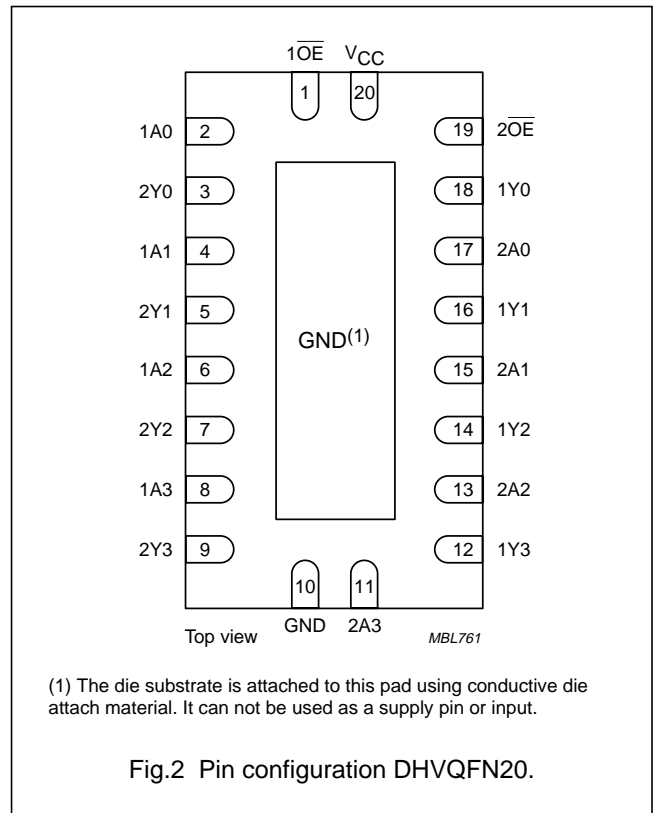
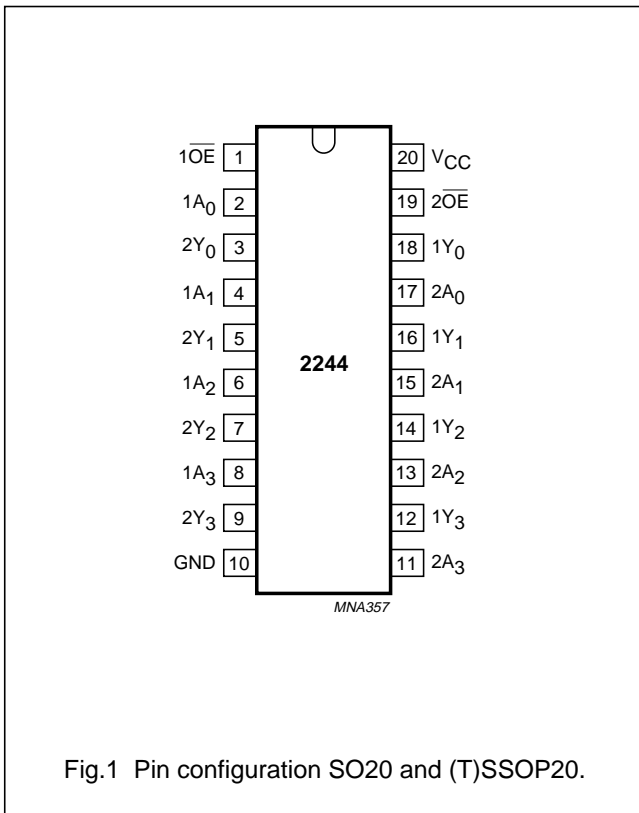
## PINNING

PIN	SYMBOL	DESCRIPTION
1	$\overline{1OE}$	output enable input (active LOW)
2	1A0	data input
3	2Y0	bus output
4	1A1	data input
5	2Y1	bus output
6	1A2	data input
7	2Y2	bus output
8	1A3	data input
9	2Y3	bus output
10	GND	ground (0 V)

PIN	SYMBOL	DESCRIPTION
11	2A3	data input
12	1Y3	data output
13	2A2	data input
14	1Y2	data output
15	2A1	data input
16	1Y1	data output
17	2A0	data input
18	1Y0	data output
19	$\overline{2OE}$	output enable input (active LOW)
20	$V_{CC}$	supply voltage

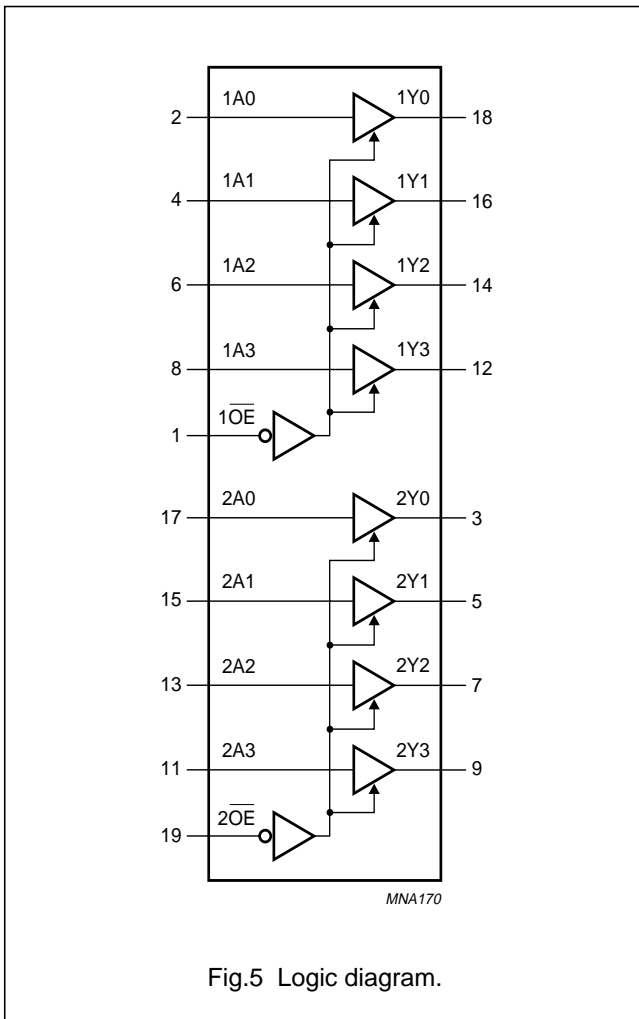
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**RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>CC</sub>	supply voltage	for maximum speed performance	2.7	3.6	V
		for low-voltage applications	1.2	3.6	V
V <sub>I</sub>	input voltage		0	5.5	V
V <sub>O</sub>	output voltage	output HIGH or LOW state	0	V <sub>CC</sub>	V
		output 3-state	0	5.5	V
T <sub>amb</sub>	operating ambient temperature		-40	+125	°C
t <sub>r</sub> , t <sub>f</sub>	input rise and fall times	V <sub>CC</sub> = 1.2 V to 2.7 V	0	20	ns/V
		V <sub>CC</sub> = 2.7 V to 3.6 V	0	10	ns/V

**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>CC</sub>	supply voltage		-0.5	+6.5	V
I <sub>IK</sub>	input diode current	V <sub>I</sub> < 0 V	-	-50	mA
V <sub>I</sub>	input voltage	note 1	-0.5	+6.5	V
I <sub>OK</sub>	output diode current	V <sub>O</sub> > V <sub>CC</sub> or V <sub>O</sub> < 0 V	-	±50	mA
V <sub>O</sub>	output voltage	output HIGH or LOW state; note 1	-0.5	V <sub>CC</sub> + 0.5	V
		output 3-state; note 1	-0.5	+6.5	V
I <sub>O</sub>	output source or sink current	V <sub>O</sub> = 0 V to V <sub>CC</sub>	-	±50	mA
I <sub>CC</sub> , I <sub>GND</sub>	V <sub>CC</sub> or GND current		-	±100	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	power dissipation	T <sub>amb</sub> = -40 °C to +125 °C; note 2	-	500	mW

**Notes**

- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- For SO20 packages: above 70 °C derate linearly with 8 mW/K.  
For SSOP20 and TSSOP20 packages: above 60 °C derate linearly with 5.5 mW/K.  
For DHVQFN20 packages: above 60 °C derate linearly with 4.5 mW/K.

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**DC CHARACTERISTICS**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP. <sup>(1)</sup>	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 °C to +85 °C</b>							
V <sub>IH</sub>	HIGH-level input voltage		1.2	V <sub>CC</sub>	–	–	V
			2.7 to 3.6	2.0	–	–	V
V <sub>IL</sub>	LOW-level input voltage		1.2	–	–	0	V
			2.7 to 3.6	–	–	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = -100 $\mu$ A	2.7 to 3.6	V <sub>CC</sub> - 0.2	V <sub>CC</sub>	–	V
		I <sub>O</sub> = -6 mA	2.7	V <sub>CC</sub> - 0.5	–	–	V
		I <sub>O</sub> = -12 mA	3.0	V <sub>CC</sub> - 0.8	–	–	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 100 $\mu$ A	2.7 to 3.6	–	0	0.2	V
		I <sub>O</sub> = 6 mA	2.7	–	–	0.4	V
		I <sub>O</sub> = 12 mA	3.0	–	–	0.55	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND	3.6	–	$\pm$ 0.1	$\pm$ 5	$\mu$ A
I <sub>OZ</sub>	3-state output OFF-state current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = 5.5 V or GND	3.6	–	0.1	$\pm$ 10	$\mu$ A
I <sub>off</sub>	power off leakage supply	V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0.0	–	0.1	$\pm$ 10	$\mu$ A
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A	3.6	–	0.1	10	$\mu$ A
$\Delta$ I <sub>CC</sub>	additional quiescent supply current per pin	V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0 A	2.7 to 3.6	–	5	500	$\mu$ A

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		OTHER	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 °C to +125 °C</b>							
V <sub>IH</sub>	HIGH-level input voltage		1.2	V <sub>CC</sub>	–	–	V
			2.7 to 3.6	2.0	–	–	V
V <sub>IL</sub>	LOW-level input voltage		1.2	–	–	0	V
			2.7 to 3.6	–	–	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = -100 $\mu$ A	2.7 to 3.6	V <sub>CC</sub> - 0.3	–	–	V
		I <sub>O</sub> = -6 mA	2.7	V <sub>CC</sub> - 0.65	–	–	V
		I <sub>O</sub> = -12 mA	3.0	V <sub>CC</sub> - 1	–	–	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 100 $\mu$ A	2.7 to 3.6	–	–	0.3	V
		I <sub>O</sub> = 6 mA	2.7	–	–	0.6	V
		I <sub>O</sub> = 12 mA	3.0	–	–	0.8	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND	3.6	–	–	$\pm$ 20	$\mu$ A
I <sub>OZ</sub>	3-state output OFF-state current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = 5.5 V or GND	3.6	–	–	$\pm$ 20	$\mu$ A
I <sub>off</sub>	power off leakage supply	V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0.0	–	–	$\pm$ 20	$\mu$ A
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A	3.6	–	–	40	$\mu$ A
$\Delta$ I <sub>CC</sub>	additional quiescent supply current per pin	V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0 A	2.7 to 3.6	–	–	5000	$\mu$ A

**Note**

1. All typical values are measured at V<sub>CC</sub> = 3.3 V and T<sub>amb</sub> = 25 °C.



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**AC CHARACTERISTICS**GND = 0 V;  $t_r = t_f \leq 2.5$  ns.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP. <sup>(1)</sup>	MAX.	UNIT
		WAVEFORMS	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 °C to +85 °C</b>							
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay nAn to nYn	see Figs 6 and 8	1.2	–	35	–	ns
			2.7	1.5	3.8	6.4	ns
			3.0 to 3.6	1.5	3.1	5.5	ns
t <sub>PZH</sub> /t <sub>PZL</sub>	3-state output enable time n $\overline{OE}$ to nYn	see Figs 7 and 8	1.2	–	38	–	ns
			2.7	1.5	5.0	8.1	ns
			3.0 to 3.6	1.0	3.9	7.1	ns
t <sub>PHZ</sub> /t <sub>PLZ</sub>	3-state output disable time n $\overline{OE}$ to nYn	see Figs 7 and 8	1.2	–	9.0	–	ns
			2.7	1.5	5.0	6.4	ns
			3.0 to 3.6	1.5	2.8	5.4	ns
t <sub>sk(0)</sub>	skew	note 2		–	–	1.0	ns
<b>T<sub>amb</sub> = -40 °C to +125 °C</b>							
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay nAn to nYn	see Figs 6 and 8	1.2	–	–	–	ns
			2.7	1.5	–	8.0	ns
			3.0 to 3.6	1.5	–	7.0	ns
t <sub>PZH</sub> /t <sub>PZL</sub>	3-state output enable time n $\overline{OE}$ to nYn	see Figs 7 and 8	1.2	–	–	–	ns
			2.7	1.5	–	10.5	ns
			3.0 to 3.6	1.0	–	9.0	ns
t <sub>PHZ</sub> /t <sub>PLZ</sub>	3-state output disable time n $\overline{OE}$ to nYn	see Figs 7 and 8	1.2	–	–	–	ns
			2.7	1.5	–	8.0	ns
			3.0 to 3.6	1.5	–	7.0	ns
t <sub>sk(0)</sub>	skew	note 2		–	–	1.5	ns

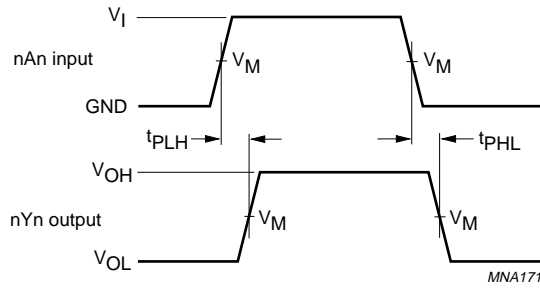
**Notes**

1. Typical values are measured at nominal V<sub>CC</sub> and T<sub>amb</sub> = 25 °C.
2. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

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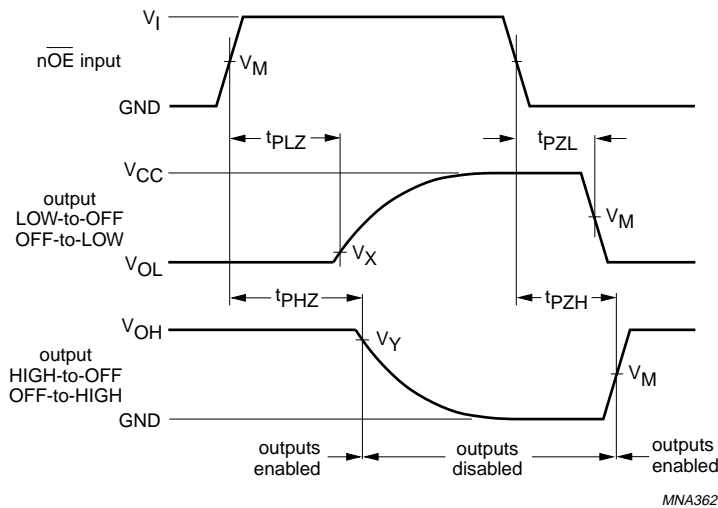
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AC WAVEFORMS



$V_M = 1.5\text{ V}$  at  $V_{CC} \geq 2.7\text{ V}$ ;  
 $V_M = 0.5 \times V_{CC}$  at  $V_{CC} < 2.7\text{ V}$ ;  
 $V_{OL}$  and  $V_{OH}$  are typical output voltage drop that occur with the output load.

Fig.6 The input nAn to output nYn propagation delays.



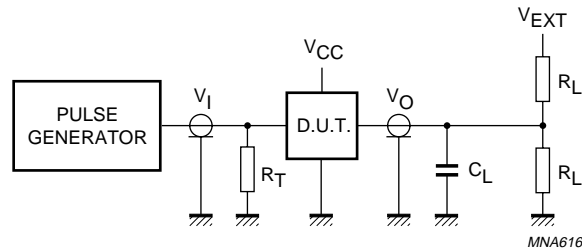
$V_M = 1.5\text{ V}$  at  $V_{CC} \geq 2.7\text{ V}$ ;  
 $V_M = 0.5 \times V_{CC}$  at  $V_{CC} < 2.7\text{ V}$ ;  
 $V_X = V_{OL} + 0.3\text{ V}$  at  $V_{CC} \geq 2.7\text{ V}$ ;  
 $V_X = V_{OL} + 0.1\text{ V}$  at  $V_{CC} < 2.7\text{ V}$ ;  
 $V_Y = V_{OH} - 0.3\text{ V}$  at  $V_{CC} \geq 2.7\text{ V}$ ;  
 $V_Y = V_{OH} - 0.1\text{ V}$  at  $V_{CC} < 2.7\text{ V}$ .

$V_{OL}$  and  $V_{OH}$  are typical output voltage drop that occur with the output load.

Fig.7 3-state enable and disable times.

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$V_{CC}$	$V_I$	$C_L$	$R_L$	$V_{EXT}$		
				$t_{PLH}/t_{PHL}$	$t_{PZH}/t_{PHZ}$	$t_{PZL}/t_{PLZ}$
1.2 V	$V_{CC}$	50 pF	500 $\Omega^{(1)}$	open	GND	$2 \times V_{CC}$
2.7 V	2.7 V	50 pF	500 $\Omega$	open	GND	$2 \times V_{CC}$
3.0 V to 3.6 V	2.7 V	50 pF	500 $\Omega$	open	GND	$2 \times V_{CC}$

**Note**

- The circuit performs better when  $R_L = 1000 \Omega$ .

Definitions for test circuits:

$R_L$  = Load resistor.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to the output impedance  $Z_o$  of the pulse generator.

Fig.8 Load circuitry for switching times.

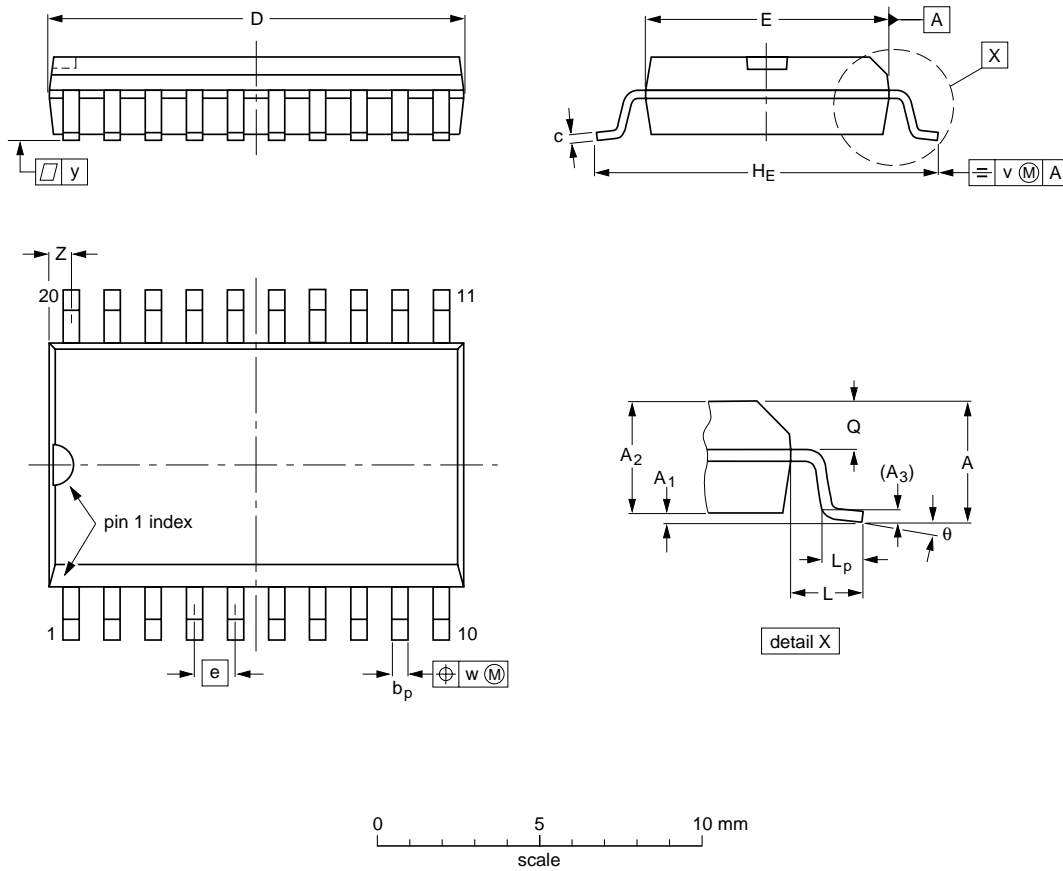
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PACKAGE OUTLINES

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

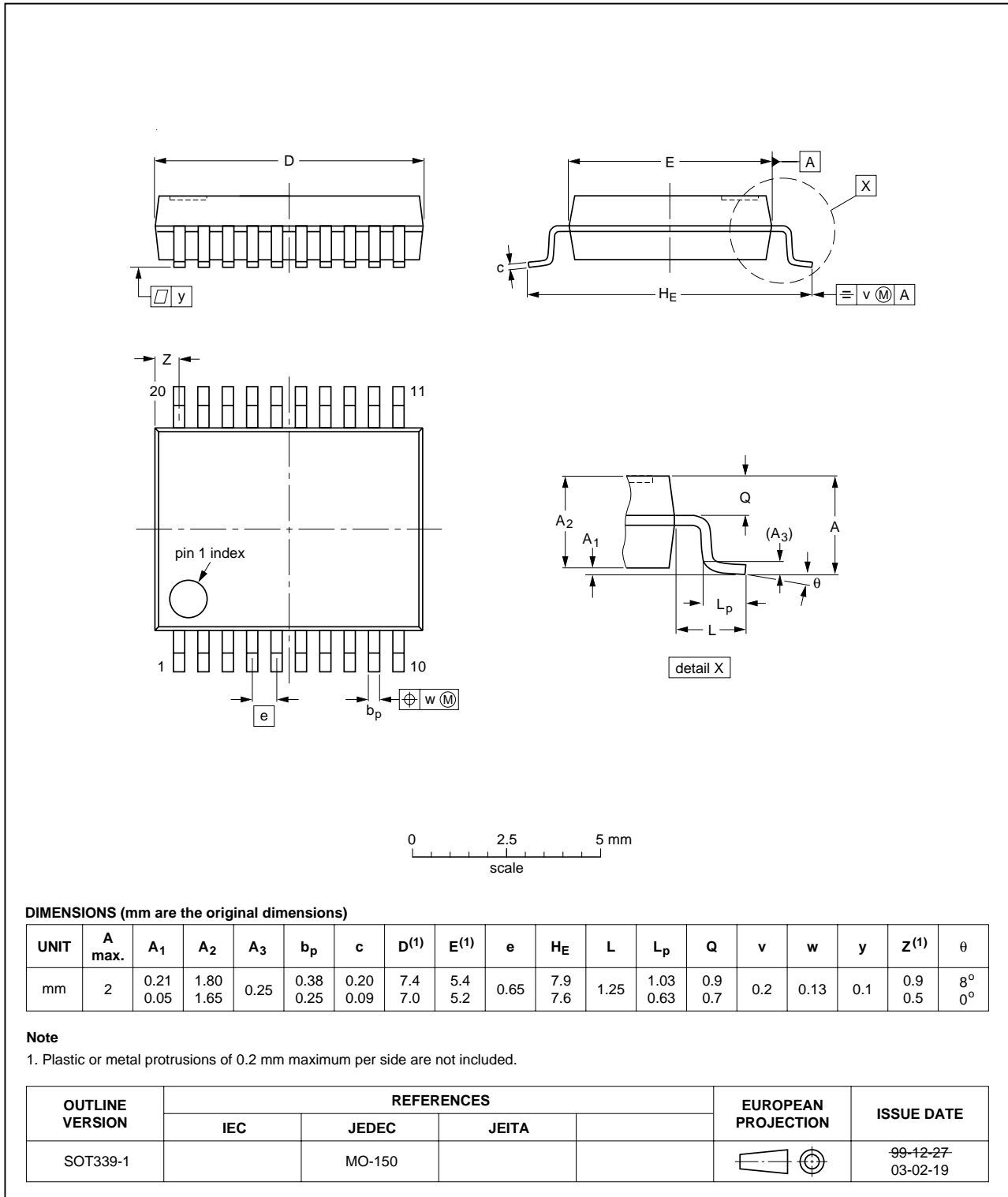
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT163-1	075E04	MS-013			99-12-27 03-02-19

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SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

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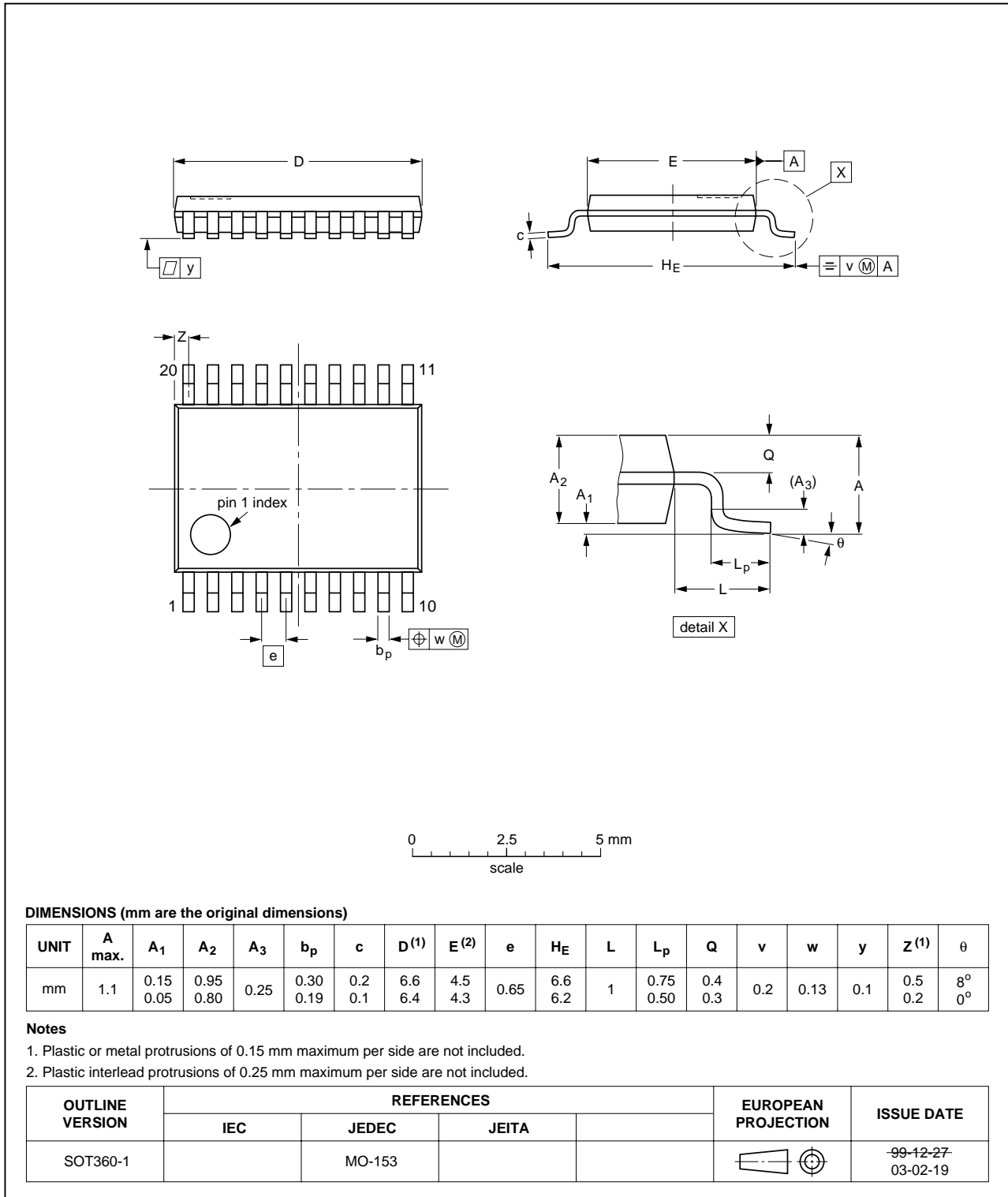


Octal buffer/line driver; with 30 Ω series termination resistors; 5 V tolerant input/output; 3-state

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TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

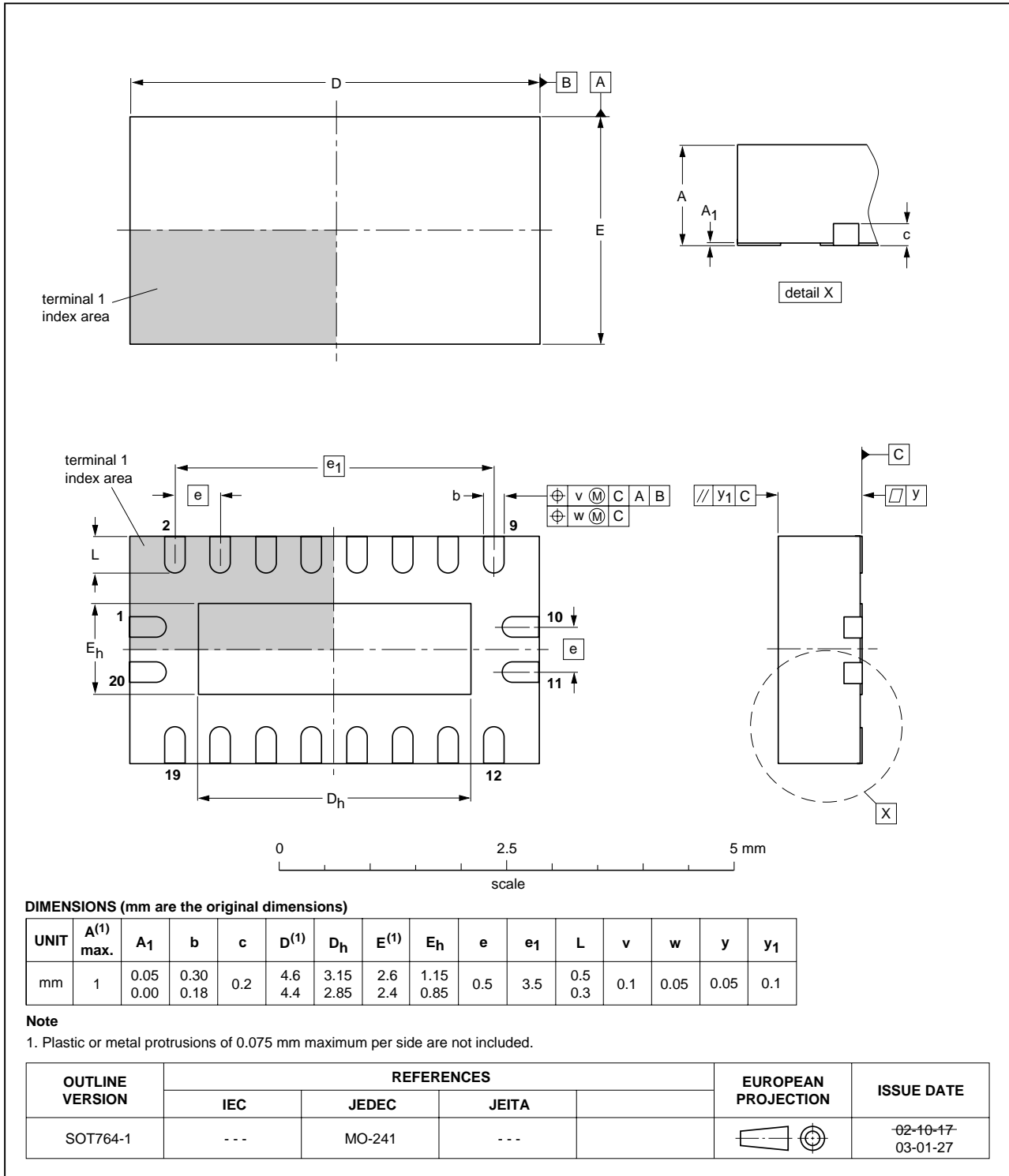


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DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm

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# Octal buffer/line driver; with 30 $\Omega$ series termination resistors; 5 V tolerant input/output; 3-state

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## DATA SHEET STATUS

LEVEL	DATA SHEET STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)(3)</sup>	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

## Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

## DEFINITIONS

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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